UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/550,598	04/17/2000	Hisashi Ohtani	0756-2119	1223

7590 05/06/2002

Nixon Peabody LLP
Suite 800
8180 Greensboro Drive
McLean, VA 22102

EXAMINER
CAO, PHAT X

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/550,598	Applicant(s) Ohtani et al.
	Examiner Phat X. Cao	Art Unit 2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jan 28, 2002* .

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-12, 14, 15, 18, and 20-29* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-12, 14, 15, 18, and 20-29* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
18) ☐ Interview Summary (PTO-413) Paper No(s). _____
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

1. The cancellation of claims 13, 16-17 and 19 in Paper No. 10 is acknowledged.

Claim Rejections - 35 USC § 112

2. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 is unclear because Zinc oxide, aluminum flakes and nickel flakes are not "organic resin" as claimed in the base claim 1.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5, 7, 9, 14, 18, 20-26, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jun (US. 6,043,149) in view of Fukunaga et al (US. 5,706,064).

With respect to claims 1, 5, 7, 9, and 27-29, Jun ('149), in Figs. 3a-3e, discloses a method for producing a semiconductor device comprising: forming a first conductive layer 32; forming an insulating layer 33 over the first conductive layer; forming an opening 34 in the insulating layer to

expose the first conductive layer 32 at a bottom of the opening; forming an embedded conductive layer 35a to cover the insulating layer and the opening; polishing the embedded conductive layer 35a by employing a chemical mechanical polishing (column 5, lines 18-21); and forming a second conductive layer 36 on the insulating layer 33 and the embedded conductive layer 35a.

Jun ('149) does not disclose that the embedded conductive layer comprises a same organic resin as the resin of the interlayer insulating film.

However, Fukunaga teaches in Fig. 17 the obviousness of forming an embedded conductive layer 411b comprising a same resin as the resin of the interlayer insulating film 413 (column 19, lines 27-35 and column 42, lines 50-52), wherein the embedded conductive layer 411b comprises an organic resin film made of carbon (column 20, lines 36-48) or polymer (column 26, lines 54-61). Accordingly, it would have been obvious to apply the contact structure of Jun in Fukunaga's display device with the embedded conductive layer and the interlayer insulating film having the resin as set forth above, in order to provide a substrate for a display device which can be used in liquid crystal in a high speed response mode and achieves a low price, as taught by Fukunaga (column 1, lines 55-59).

With respect to claims 14 and 18, Fukunaga further teaches the obviousness of forming the embedded conductive layer 411b made of inorganic oxide conductive layer of ITO or ZnO (column 30, lines 43-46 and column 5, lines 66-67 through column 6, lines 1-3).

With respect to claims 20-26, Fukunaga also teaches (column 1, lines 5-30) that because the liquid crystal display device has high image quality and can be used as switching elements, this

kind of display device has been widely used as a display device in a personal computer, television or the like. Accordingly, it would have been obvious to apply the display device of Fukunaga to a cellular phone, a camcorder, etc., because it is an intended use.

5. Claims 1, 5, 7, 9, 14, 18, and 20-29 rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al (US. 6,081,305) in view of Fukunaga et al (US. 5,706, 064).

With respect to claims 1, 5, 7, 9, and 27-29, Sato (Fig. 2) discloses a method for producing a semiconductor device comprising: forming a first conductive layer 164; forming an insulating layer 170 over the first conductive layer; forming an opening in the insulating layer to expose the first conductive layer 164 at a bottom of the opening; forming an embedded conductive layer 171 to cover the insulating layer and the opening; etching the embedded conductive layer to expose a portion of the insulating layer 170; and forming a reflective pixel electrode 181 on the insulating layer 170 and the embedded conductive layer 171.

Sato does not disclose that the embedded conductive layer comprises a same organic resin as the resin of the interlayer insulating film.

However, Fukunaga teaches in Fig. 17 the obviousness of forming an embedded conductive layer 411b comprising a same resin as the resin of the interlayer insulating film 413 (column 19, lines 27-35 and column 42, lines 50-52), wherein the embedded conductive layer 411b comprises an organic resin film made of carbon (column 20, lines 36-48) or polymer (column 26, lines 54-61). Accordingly, it would have been obvious to form the embedded conductive layer and the interlayer insulating film with the resin as set forth above, in order to

provide a substrate for a display device which can be used in liquid crystal in a high speed response mode and achieves a low price, as taught by Fukunaga (column 1, lines 55-59).

With respect to claims 14 and 18, Fukunaga further teaches the obviousness of forming the embedded conductive layer 411b made of inorganic oxide conductive layer of ITO or ZnO (column 30, lines 43-46 and column 5, lines 66-67 through column 6, lines 1-3).

With respect to claims 20-26, Fukunaga also teaches (column 1, lines 5-30) that because the liquid crystal display device has high image quality and can be used as switching elements, this kind of display device has been widely used as a display device in a personal computer, television or the like. Accordingly, it would have been obvious to apply the display device of Fukunaga to a cellular phone, a camcorder, etc., because it is an intended use.

6. Claims 3, 6, 8, 10, and 20-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (US. 5,990,542) in view of Fukunaga et al (US. 5,706,064).

With respect to claims 3, 6, 8, and 10, Yamazaki (Fig. 2B) discloses a method for producing a semiconductor device comprising: forming an active layer of transistor; forming an insulating layer over the active layer; forming an opening in the insulating layer to expose a portion of the active layer at a bottom of the opening; forming an embedded conductive layer made of ITO to cover the insulating layer and the opening wherein the embedded conductive layer contacts the active layer in the opening; forming a transparent conductive layer 121 on the embedded conductive layer; patterning the transparent conductive layer 121 to form a transparent pixel electrode (column 6, lines 7-9).

Yamazaki does not disclose the embedded conductive layer made of carbonblack.

However, Fukunaga teaches the obviousness of forming the embedded conductive layer 411b made of carbonblack (column 20, lines 36-42) or made of ITO or ZnO (column 5, lines 66-67 through column 6, lines 1-3). Accordingly, it would have been obvious to form the embedded conductive layer with the materials as set forth above, in order to provide a substrate for a display device which can be used in liquid crystal in a high speed response mode and achieves a low price, as taught by Fukunaga (column 1, lines 55-59).

With respect to claims 20-26, Fukunaga also teaches (column 1, lines 5-30) that because the liquid crystal display device has high image quality and can be used as switching elements, this kind of display device has been widely used as a display device in a personal computer, television or the like. Accordingly, it would have been obvious to apply the display device of Fukunaga to a cellular phone, a camcorder, etc., because it is an intended use.

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Jun (US. 6,043,149) and Fukunaga et al.

As discussed above, Yamazaki (Fig. 2B) substantially reads on above claim, except that it does not disclose the embedded conductive layer is polished by CMP before forming the transparent electrode.

However, Jun ('149), in Fig. 3e, teaches the obviousness of polishing the embedded conductive layer 35 by CMP (column 5, lines 18-21) before forming the upper electrode. Accordingly, it would have been obvious to form the embedded conductive layer and the

transparent pixel electrode of Yamazaki with the process as set forth above for improving step coverage and for preventing a recess formation in the contact hole, as taught by Jun (column 4, lines 39-43 and column 5, lines 18-21).

8. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jun (US. 5,948,705) in view of Kobayashi et al (US. 6,221,140).

With respect to claim 2, Jun, in Figs. 3A - 3E, discloses a method for producing a semiconductor device comprising: a step of forming a first conductive layer 33; a step of forming an insulating layer 34 over the first conductive layer; a step of forming an opening 35 in the insulating layer 34 to expose the first conductive layer 33 at a bottom of the opening; a step of forming an embedded conductive layer 36 to cover the insulating layer and the opening; a step of etching the embedded conductive layer 36 to make a sate in that only the opening is filled with the embedded conductive layer 36; and a step of forming a second conductive layer 38 on the insulating layer and the embedded conductive layer.

With respect to claim 4, Jun further discloses in Figs. 4A - 4E another method for producing a semiconductor device comprising all the steps recited in the claimed invention, including a step of etching the embedded conductive layer 46' by using the second conductive layer 48 as a mask in a self-alignment manner (see Figs. 4D - 4E and column 7, lines 25-30).

Jun ('705) does not disclose the conductive layer 46 is made of an oxide conductive layer and is formed by a spin coating method.

However, Kobayashi et al teach in column 2, lines 34-48 the obviousness of forming an oxide conductive layer by a spin coating method to cover the substrate and the opening. Accordingly, it would have been obvious to form the conductive layer 46 of Jun with the material and the method as set forth above, because according to Jun a method of spin coating of an oxide conductive layer on a substrate is known for reducing in manufacturing cost (see column 2, lines 24-33).

9. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jun ('705) and Kobayashi et al as applied to claim (2,4) above, and further in view of Fukunaga et al.

Neither Jun nor Kobayashi et al discloses the embedded conductive layer made of materials as claimed.

However, Fukunaga et al teach in Fig. 17 the obviousness of forming an embedded conductive layer 411b made of inorganic oxide conductive layer of ITO or ZnO (column 5, lines 66-67 through column 6, lines 1-3), or made of organic conductive layer of carbon (column 20, lines 36-37), or polymer (column 26, lines 54-61). Accordingly, it would have been obvious to form the embedded conductive layer of the above combination with the materials as set forth above, because according to Fukunaga et al, these materials would provide a low price and a high speed response mode for LCD (column 1, lines 55-59).

Response to Arguments

10. Applicant's arguments with respect to the claimed invention have been considered but are moot in view of the new ground(s) of rejection.

With respect to the combination of Jun ('705) and Kobayashi, Applicant argues that "there is no suggestion in Kobayashi to form an oxide conductive layer as the plug..."

It should be noted that the rejection is not based on anticipation, but rather, is based on obviousness. The Examiner relies on the combined teachings at Jun and Kobayashi. Kobayashi is not relied on for teaching a method of forming a conductive plug. Jun discloses a method of forming a conductive plug. Kobayashi is relied on for showing that it was known to forming an oxide conductive layer on the substrate by a spin coating for reduction in manufacturing cost (column 2, lines 27-33). Furthermore, Kobayashi does suggest the forming of the oxide conductive layer in the opening because in column 2, lines 36-41, Kobayashi discloses that "after a mask having an opening having a predetermined pattern is formed on the substrate, the organic metal compound solution is coated on the substrate by dipping, spin-coating, spray-coating, or the like, and the coated film is heated and decomposed to obtain a metal or a metal oxide." [underline added].

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (703) 308-4917. The Examiner can normally be reached on Monday through Thursday. If attempts to reach the Examiner by telephone are unsuccessfully, the Examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. Group 2800 fax number is (703) 308-7722 or (703) 308-7724.

PC
May 3, 2002

PHAT X. CAO
PRIMARY EXAMINER